

Remarks

Favorable reconsideration of this application is requested in view of the above amendments and the following remarks. Claims 20-21 have been newly added. Claims 1-6 and 19-21 remain pending in the present application.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Londa in view of Clayton and Panchou, further in view of Bertin et al. This rejection is respectfully traversed.

The claimed invention discloses a one-piece chip-mounting member (1) with opposite surfaces (10, 11), each of which has a respective semiconductor chip (2) mounted thereon by means of a dielectric tape (4). The dielectric tape (4) is formed with a plurality of holes (40) to receive contact balls (5) for establishing electrical connection between contact pads (21) on the respective semiconductor chip (2) and circuit traces (12) on the respective surface (10, 11) of the chip-mounting member (1). The circuit traces (12) on the surfaces (10, 11) of the chip-mounting member (1) are coupled electrically by means of plated through holes (14) in the chip-mounting member (1). Solder balls (3) are formed on one of the surfaces (10, 11) of the chip-mounting member (1), whereby the circuit traces (12) on two chip-mounting member (1) can be connected electrically via the solder balls (3) on one of the chip-mounting members (1) to form a semiconductor chip module stack.

In contrast, Londa discloses a chip-mounting member including first and second substrates (12, 22) and a conductive plane (30) disposed therebetween. Each of the first and second substrates (12, 22) is formed with an opening (18, 28) so that first and second electronic devices (36, 40) can be secured on opposite surfaces of the conductive plane (30) within the opening (18, 28) in the respective one of the first and second substrates (12, 22). Because the bond wires (102a, 102b, 102c, 102d) are used to couple electrically the first and second electronic devices (36, 40) to circuit layers (20, 27) on the first and second substrates (12, 22), it is necessary to form the first and second substrates (12, 22) with the openings (18, 28) to reduce the overall profile of the electronic device package. See Figure 2 of Londa. Further, Figure 4 of Londa illustrates a chip-mounting member formed of first

and second substrates (312, 328). The first substrate (312) is formed with a cavity (318), and a first electronic device (326) is secured to the first substrate (312) in the cavity (318). Bond wires (402a, 402b) electrically couple the first electronic device (326) to a circuit layer (320) on the first substrate (312). The second substrate (328) is formed with an opening (408) and a thermally conductive plane (410) on one side opposite to the first substrate (312). A second electronic device (336) is secured to the plane (410) within the opening (408), and is coupled electrically to a circuit layer (322) on the second substrate (328) via bond wires (402c, 402d). The circuit layers (320, 322) are coupled electrically via solder ball pads. Because of the bond wires (402a, 402b, 402c, 402d), the cavity (318) in the first substrate (312) and the opening (408) in the second substrate (328) are necessary so as to reduce the overall profile of the electronic device package. In addition, Figure 6 of Londa illustrates a chip-mounting member formed of first and second substrates (512, 524). A first electronic device (522) is secured to the first substrate (512) and is coupled electrically to a circuit layer (518) on the first substrate (512) via bond wires (616a, 616b). A second electronic device (532) is secured to the second substrate (524) and is coupled electrically to a circuit layer (530) on the second substrate (524) via bond wires (616c, 616d). The first and second substrates (512, 524) are coupled electrically via solder ball pads. The second substrate (524) is formed with a cavity (538) that confronts the first electronic device (522) to reduce the overall profile of the electronic device package.

Thus, Londa fails to disclose a one-piece chip-mounting member that has opposite surfaces, each of which has a respective semiconductor chip mounted thereon by using respective dielectric tape to bond and establish electrical connection between the chip and the circuit traces. In Londa, because bond wires are used for establishing electrical connection between electronic devices and circuit layers, the chip-mounting member formed of substrates is required to have cavities or openings to reduce the overall profile of the electronic device package. However, in the claimed invention, contact balls are used for electrically connecting the semiconductor chip and the circuit traces, and no cavities/opening is needed in the chip-mounting member. In addition, the use of two

substrates that are formed with openings/cavities and that are subsequently joined together as taught by Londa is not economical because of higher material and manufacturing costs.

Even though Clayton and Panchou teach that a dielectric tape can be used to mount an integrated circuit on a substrate and that the dielectric tape can be formed with conductors for establishing electrical connection between the integrated circuit and circuit traces on the substrate, the combination of the cited references (Londa, Clayton and Panchou) would not lead one skilled in the art to obtain a one-piece chip mounting member that does not need to be formed with cavities/openings for reducing the overall profile of the semiconductor chip module. Bertin also fails to remedy such deficiencies.

Therefore, claims 1-6 and 19 are patentable over Londa in view of Clayton and Panchou, further in view of Bertin.


Newly added claim 20 includes the limitations of claims 1-4 and have the features as discussed above, and thus claim 20 and its dependent claim 21 should be in condition for allowance.

In view of the above, it is respectfully submitted that the present application is in condition for allowance. Reconsideration of the present application and a favorable response are respectfully requested.

Respectfully submitted,

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